Compact Series Single Board Hardware Design User Guide

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Document version revision record

Version number	Release date	Revision history
V1.0	2020/03/23	Initial version

Glossary

PCB: Printed Circuit Board

BGA: Ball Grid Array

FBG: F=1.0mm ball pitch, B= Ball Grid Array, G=Pb free

MBG: M=0.8mm ball pitch, B= Ball Grid Array, G= Pb free

SSBG: S=Special S=0.5mm ball pitch, B= Ball Grid Array, G= Pb free

UWG: U=0.4mm ball pitch, W= Wafer level chip scale package, G= Pb free

LPG: L=package thickness >1.2mm, P= QFP(Quad flat package) , G= Pb free

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1. Overview

Compact Series Single Board Hardware Design User Guide is a recommended design document for the single board hardware of Compact series CPLD chips.

Please refer to "DS03001_Compact Series CPLD Device Data Sheet" for the general introduction of the Compact series CPLD, product features, resource scale, package information and the number of user IOs.

2. Power supply

(1) Voltage

Table 1 is the working voltage and temperature requirements.

Table 1 Recommended Device Operating Conditions

Symbol	Description	Minimum	Typical	Maximum
VCC[1]	External supply voltage for L-type devices	1.14 V	1.2 V	1.26 V
	External Supply Voltage for Type G/D Type Devices	2.375 V	2.5V/3.3 V	3.465 V
VCCIO[1,2]	I/O Bank Voltage	1.14 V	--	3.465 V
T_J	Commercial Grade Operating Junction Temperature	0 ℃	--	85 ℃
	Industrial Grade Operating Junction Temperature	-40 ℃	--	100 ℃

1. All power supply pins must be connected to the corresponding external power supply, and the same power supply should be connected together. For example, if VCCIO and VCC are the same voltage value, they must come from the same power supply

2. When making the board, the VCCIO pin of the unused I/O Bank should be connected to VCC

3. There is no requirement for the power-on sequence, and they can be powered on at the same time

4. The power supply ripple requirement is ±5% of the nominal voltage

Table 2 Device Power Supply Voltage Requirements

Power Supply Type / Chip model	VCC[1]	VCCIO0[1,2]	VCCIO1[1,2]	VCCIO2[1,2]	VCCIO3[1,2]	VCCIO4[1,2]	VCCIO5[1,2]
PGC1KL_UWG36	1.2 V	1.2V-3.3 V[3]	--[4]	1.2V-3.3 V	1.2V-3.3 V	--	--
PGC2KL_UWG49	1.2 V	1.2V-3.3 V	--	1.2V-3.3 V	--	--	1.2V-3.3 V
PGC2KL_SSBG256	1.2 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KL_UWG81	1.2 V	1.2V-3.3 V	--	1.2V-3.3 V	1.2V-3.3 V	--	1.2V-3.3 V
PGC4KL_SSBG256	1.2 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC1KG_LPG100	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC1KG_LPG144	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC1KG_MBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC1KG_FBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC2KG_LPG100	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC2KG_LPG144	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC2KG_MBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC2KG_FBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KD_MBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KD_MBG324	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KD_MBG332	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC4KD_MBG400	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_FBG484	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_MBG400	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_MBG256	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_MBG332	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V
PGC7KD_LPG144	2.5V/3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V	1.2V-3.3 V

1. All power supply pins must be connected to the corresponding external power supply, and the same power supply should be connected together. For example, if VCCIO and VCC are the same voltage value, they must come from the same power supply

2. The VCCIO pins of unused I/O Banks should be connected to VCC

3. 1.2V-3.3V voltage includes 1.2V, 1.5V, 1.8V, 2.5V and 3.3V, the same below

4. Indicates that the corresponding chip does not have this Bank

(2) Power consumption

Table 3 provides the measured values of the core current of different CPLD devices as a reference for PCB design, and can also be evaluated by using the power consumption evaluation software PPP. The current of BANK is related to the package, and can be evaluated by using the power consumption evaluation software PPP.

Table 3 Core Current for PGC Family Devices

Device	Resource usage	Core current
1KL	80%, System clock 125MHz	70mA
1KG	80%, System clock 150MHz	80mA
2KL	80%, System clock 125MHz	130mA
2KG	80%, System clock 150MHz	150mA
4KL	80%, System clock 125MHz	210mA
4KD	80%, System clock 150MHz	260mA
7KD	80%, System clock 150MHz	370mA

(3) Power supply routing

The power and ground wires should be short and thick, and it is recommended to design them in the form of a plane when conditions permit.

Generally speaking, decoupling should be performed between the chip's power pins and ground pins, and the decoupling capacitor should be placed as close to the chip pins as possible. Try to put a 0.1uF decoupling capacitor on each power pin, and each Bank power supply Place 1~2 10uF capacitors, 1~2 10uF capacitors or 1~2 22uF capacitors for the core power supply. The reference is shows in Figure 1.

If you want to calculate how much capacitance you need more accurately, you first need to know the maximum transient current of each power supply on the board, and then set the target impedance of the power supply in the PI (power integrity) simulation software according to the actual stacking of the PCB. Calculate whether the capacitor configuration is appropriate through simulation, and then modify the capacitor configuration in the schematic diagram in turn.

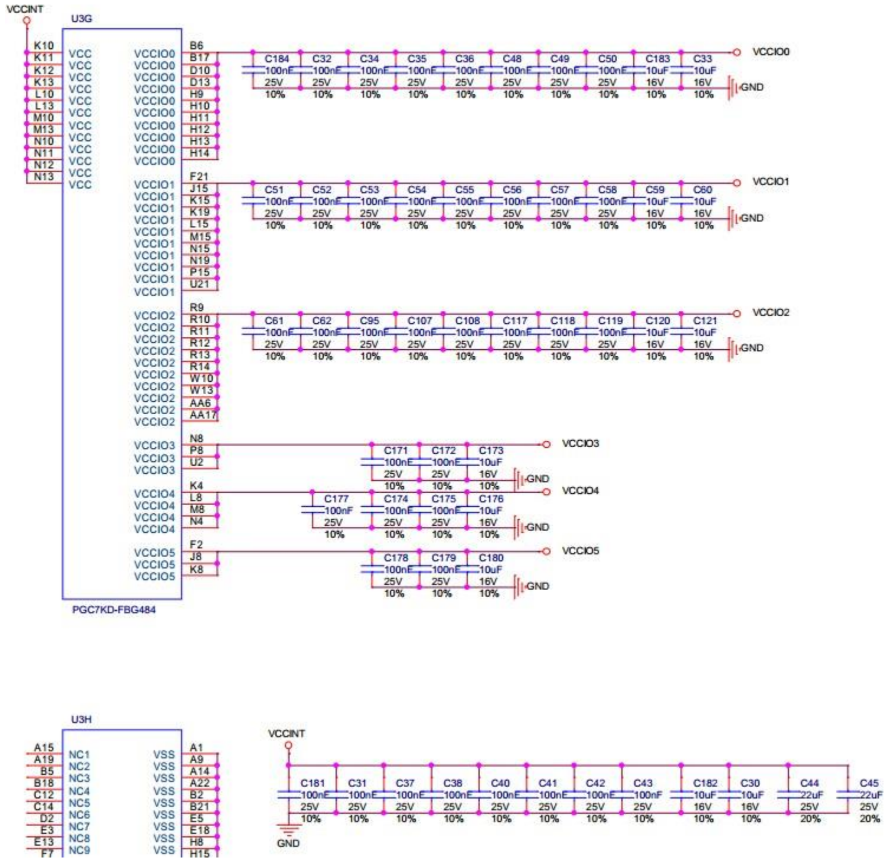


Figure 1 PGC series CPLD power supply decoupling schematic diagram

For example, if the core power supply voltage is 1.2V, the maximum transient current value estimated by the power consumption evaluation software is 1A, and the AC ripple fluctuation required by the core power supply is ±5%, that is, 60mV, then the target impedance of the core power supply is

$$60mV/1A=60m\Omega$$

Therefore, as long as the simulated power supply impedance is less than the target impedance within the maximum frequency range required by the application, the AC ripple fluctuation will be less than the required ±5%.

The required maximum frequency refers to the frequency point at which the power supply impedance will not be lower than the target impedance after adding a certain amount of decoupling capacitors. This is because the main impedance of the stray plane is the spreading inductance and the mounting inductance of the package. Generally In general, this frequency ranges from 50/60MHz up to 150/200MHz. Outside of these frequencies, it is the package and die capacitance of the selected target device that maintains power integrity.

To maintain power integrity over the entire required frequency range, the power distribution system employs power modules (VRMs), on-board discrete decoupling capacitors, and interplane capacitors (power and ground sandwich capacitors from the board stackup).

For high frequencies, decoupling with discrete capacitors is not efficient. For these frequencies, use power plane capacitors for noise decoupling.

The purpose of the power distribution system is to provide and maintain the required target constant voltage for the power and ground pins of each device. To achieve this goal efficiently, the power distribution system uses power supply (VRM), bulk capacitance and decoupling Capacitors (Decaps) and power and ground plane sandwich structures (planar capacitors). Whether these components can effectively help maintain a constant voltage under various transient load conditions depends mainly on their associated stray inductance.

As a first-order approximation, VRM can be simply equivalent to a series connection of resistors and inductors. In the low frequency range of tens of kHz, VRM is mainly a resistor with extremely low impedance, so it can meet the instantaneous current requirements at low frequencies. However, after tens of kHz, the VRM impedance is mainly inductance, which can no longer meet the transient current requirements.

On-board discrete decoupling capacitors must be able to meet low impedance requirements from tens of kHz to hundreds of MHz, depending on capacitor ESR and ESL and board mounting and spreading stray inductance. Decoupling capacitors, since stray mounting and spreading inductance will limit the effect of these capacitors, when designing a power distribution system, care must be taken to minimize the various stray inductances associated with the board design.

Commonly used PI simulation software includes Siwave from ANSYS and Sigrity from Cadence.

Figure 2 is the real picture of the capacitor placement PCB of the PGC7KD-MBG400 package.

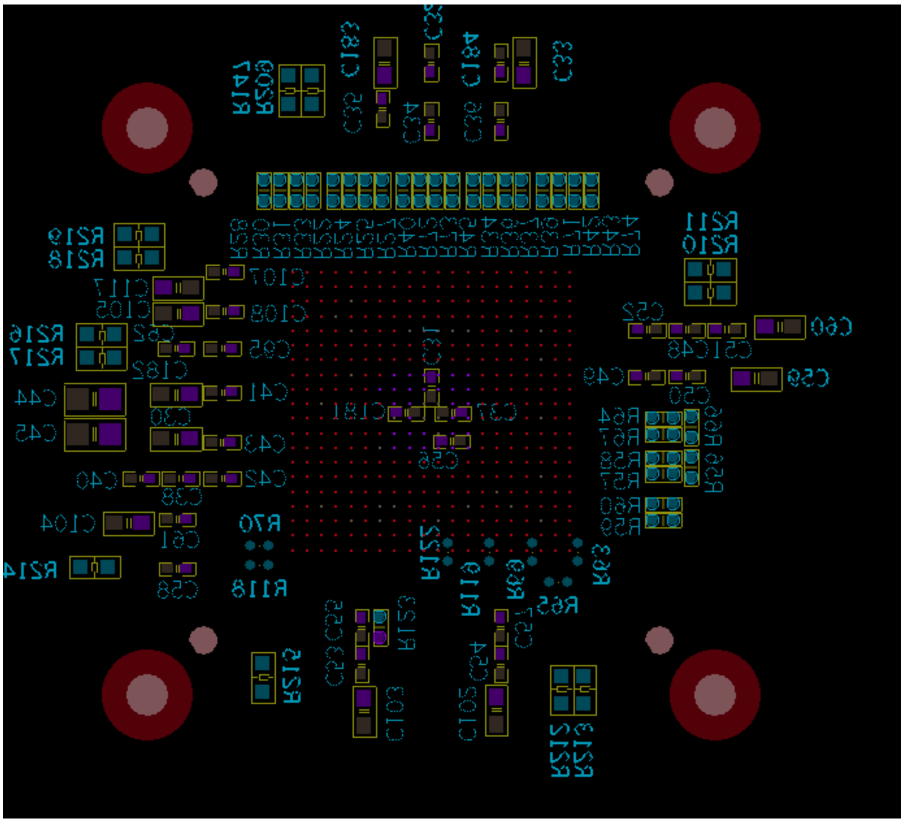


Figure 2 PGC7KD-MBG400 package capacitor placement PCB real picture

3. Packaging and FANOUT

The diameter of the BGA pad is generally designed to be the same as the diameter of the FPGA ball. In special cases, it can be 20%~25% smaller than the diameter of the FPGA ball. The Fanout reference schematic is given below.

As shown in Figure 3. The cross in the middle divides the BGA into 4 areas on average, and the solder pads in each area go out to the outside of the BGA. The position of the cross can be adjusted asymmetrically due to the need for wiring. The cross can be used for power supply in the middle layer Traces, traces with a larger line spacing, etc., are used to place filter capacitors on the bottom layer. The two outermost rows of pads can directly go out from the surface layer of the chip soldering surface; Pull it out to avoid turning inside. The power and ground wires need to be widened.

The number of traces between the surface pads should be maximized, but long traces should be avoided to prevent poor PCB processing and poor placement.

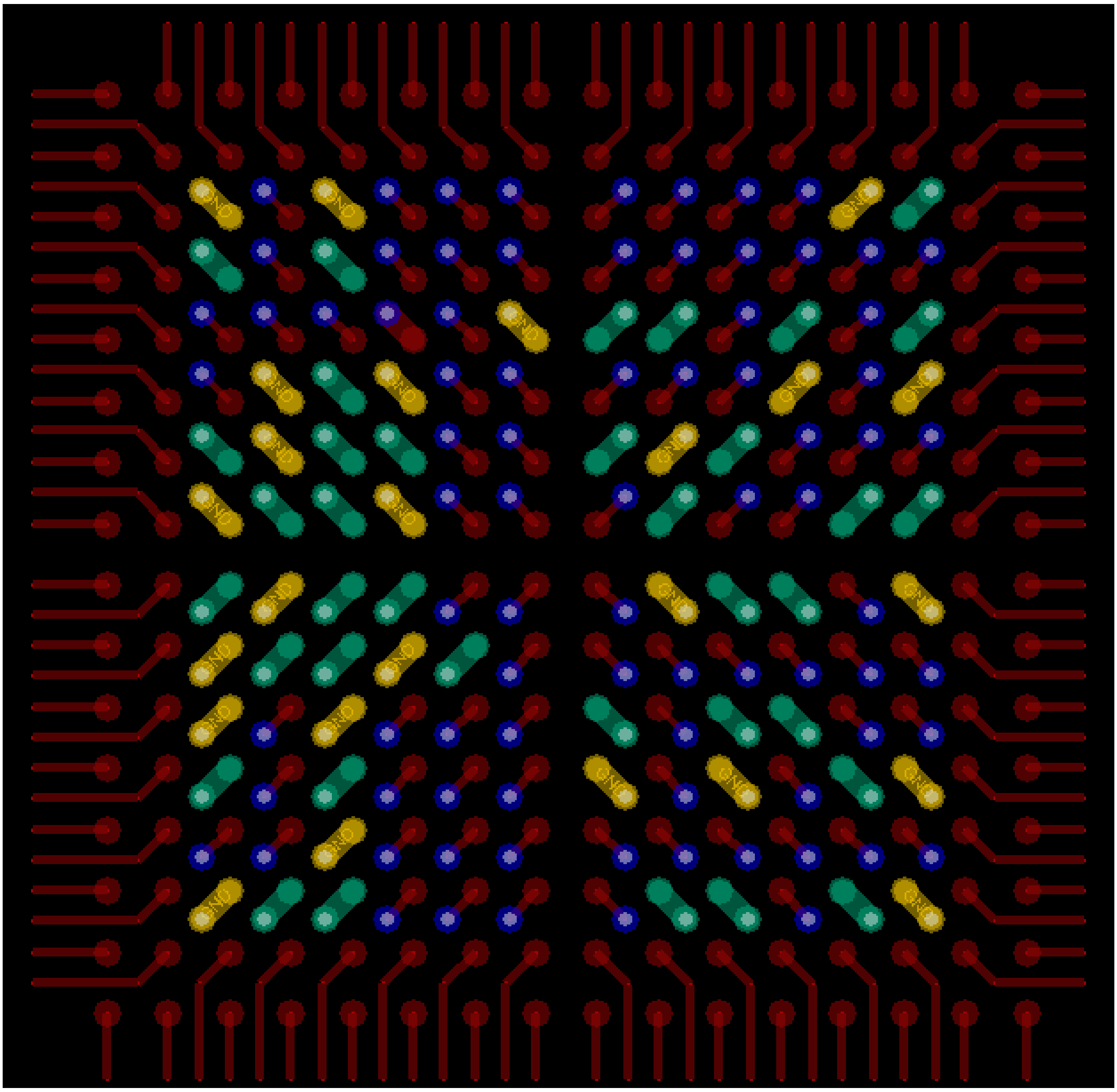


Figure 3 BGA Fanout Reference Schematic

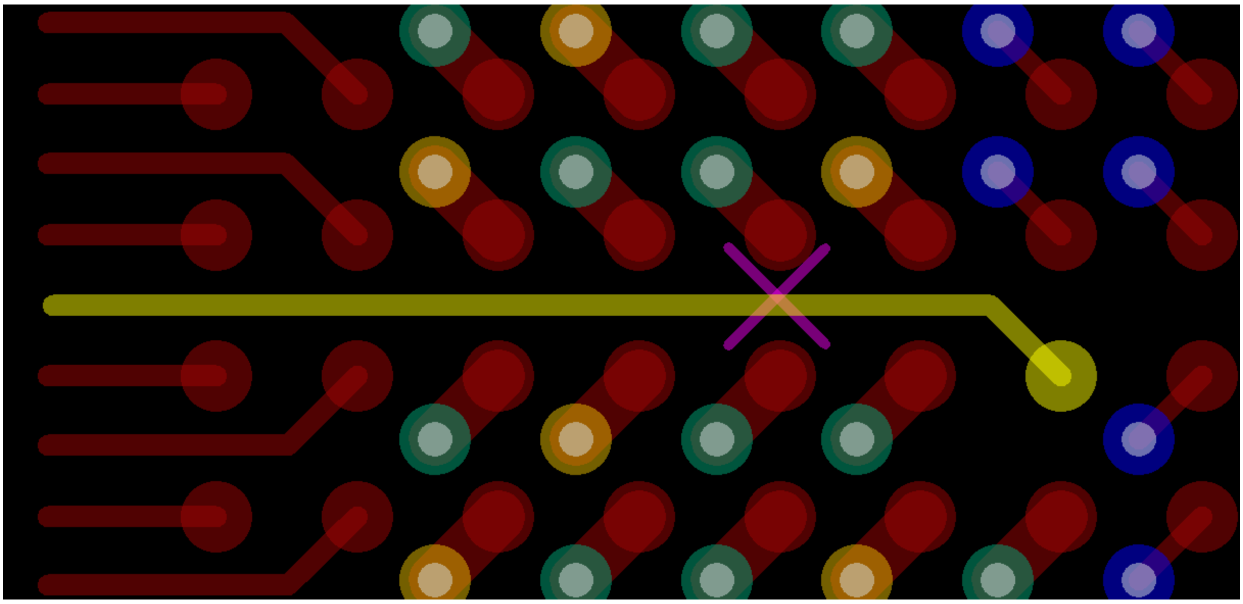


Figure 4 Schematic diagram of long traces between BGA surface pads

Long traces (yellow traces) between surface pads will increase the risk of short circuits between traces and pads, and should be avoided.

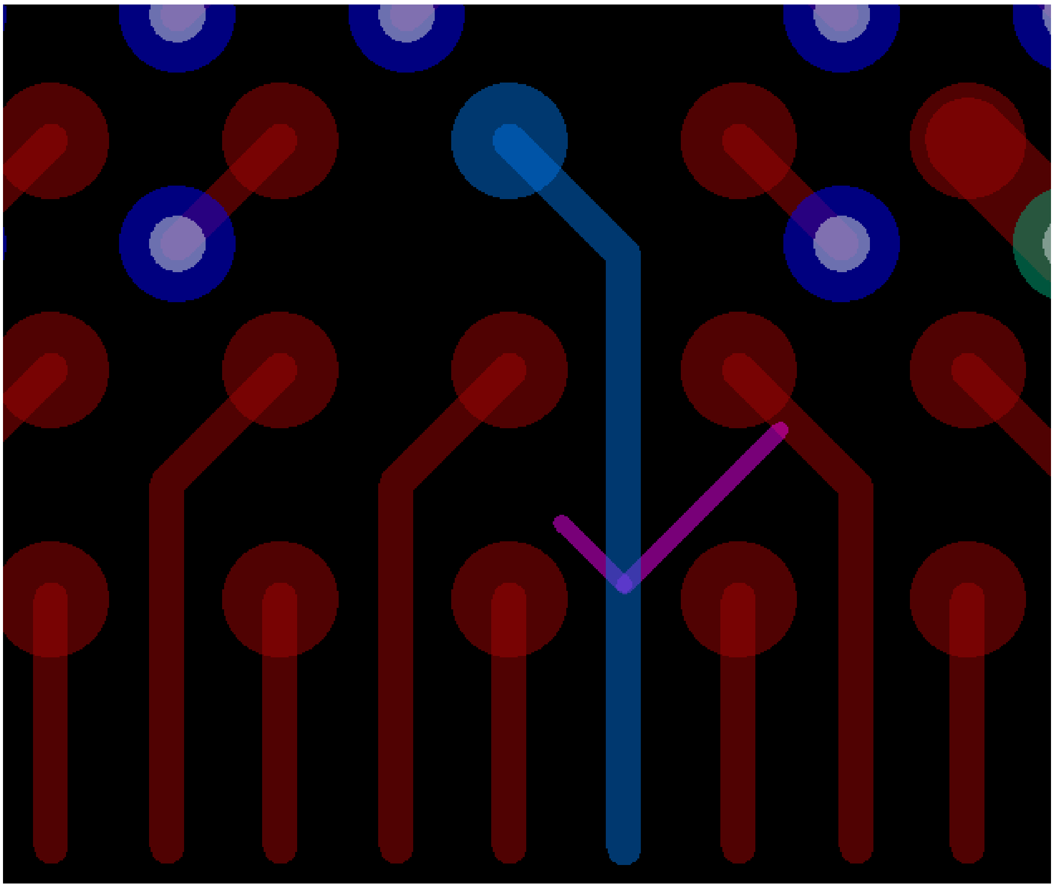


Figure 5 Schematic diagram of BGA surface wiring

Row 3 can have a pad coming out of the middle cross gap of Fanout (blue trace).

(1) FBG

There are currently two types of FBG packages for Compact series CPLDs, namely FBG256 and FBG484, with a pad pitch of 1.0mm. For specific package information, please refer to the corresponding chip package user guide of Unigroup.

Pad and via size, trace width are recommended as follows:

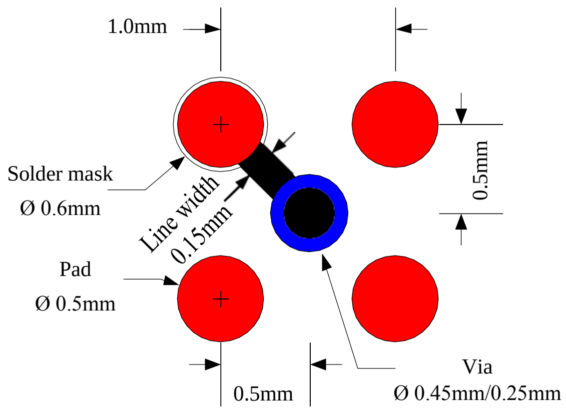


Figure 6 Schematic diagram of recommended dimensions for FBG package pads and vias

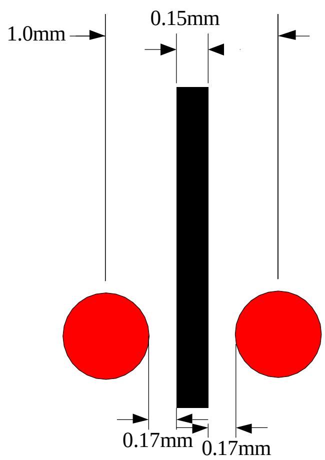


Figure 7 Schematic diagram of the recommended size of the wires between the pads of the FBG package

(2) MBG

Compact series CPLDs currently have 4 types of MBG packages, namely MBG256, MBG324, MBG332 and MBG400, with a pad pitch of 0.8mm. For specific package information, please refer to the corresponding chip package user guide of Unigroup.

Pad and via size, trace width are recommended as follows:

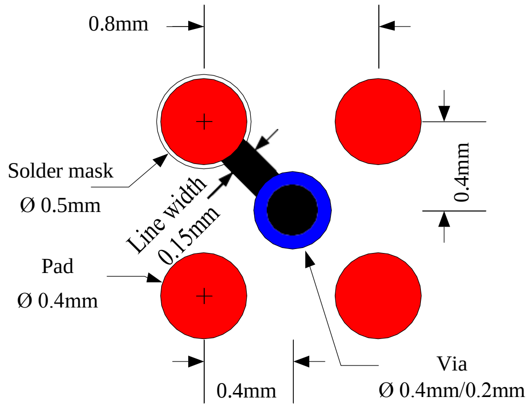


Figure 8 Schematic diagram of recommended dimensions for MBG package pads and vias

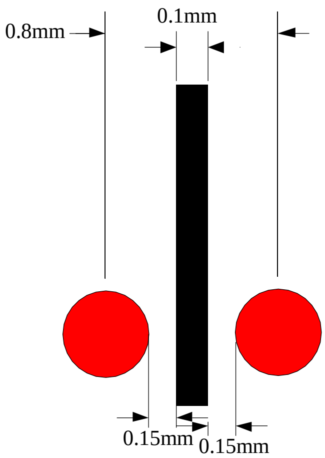


Figure 9 Schematic diagram of the recommended size of the outgoing wires between the pads of the MBG package

(3) SSBG

The Compact series CPLD currently only has one SSBG package SSBG256, with a pad pitch of 0.5mm. For specific package information, please refer to the corresponding chip package user guide of Unigroup.

The SSBG package has a small pad spacing, and the space between the pads cannot be routed. Blind buried holes are generally required in PCB design. When the number of pins used is small, if the used pin position is planned reasonably, It is possible to use only through-hole vias, the vias are punched on the pads.

Pad and via size recommendations are as follows:

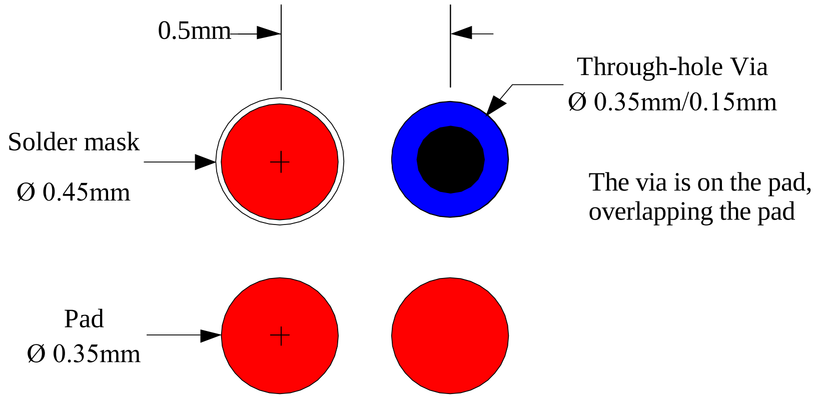


Figure 10 Schematic diagram of recommended dimensions for SSBG package pads and through-hole vias

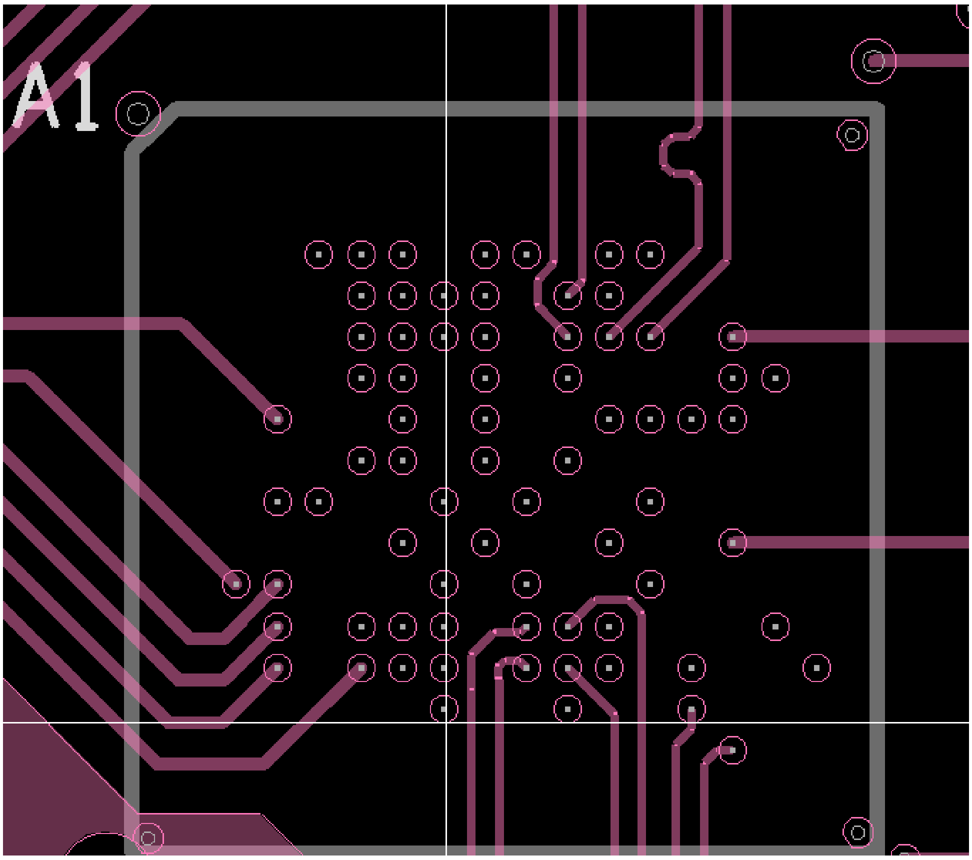


Figure 11 SSBG package corresponds to PCB middle layer wiring diagram 1

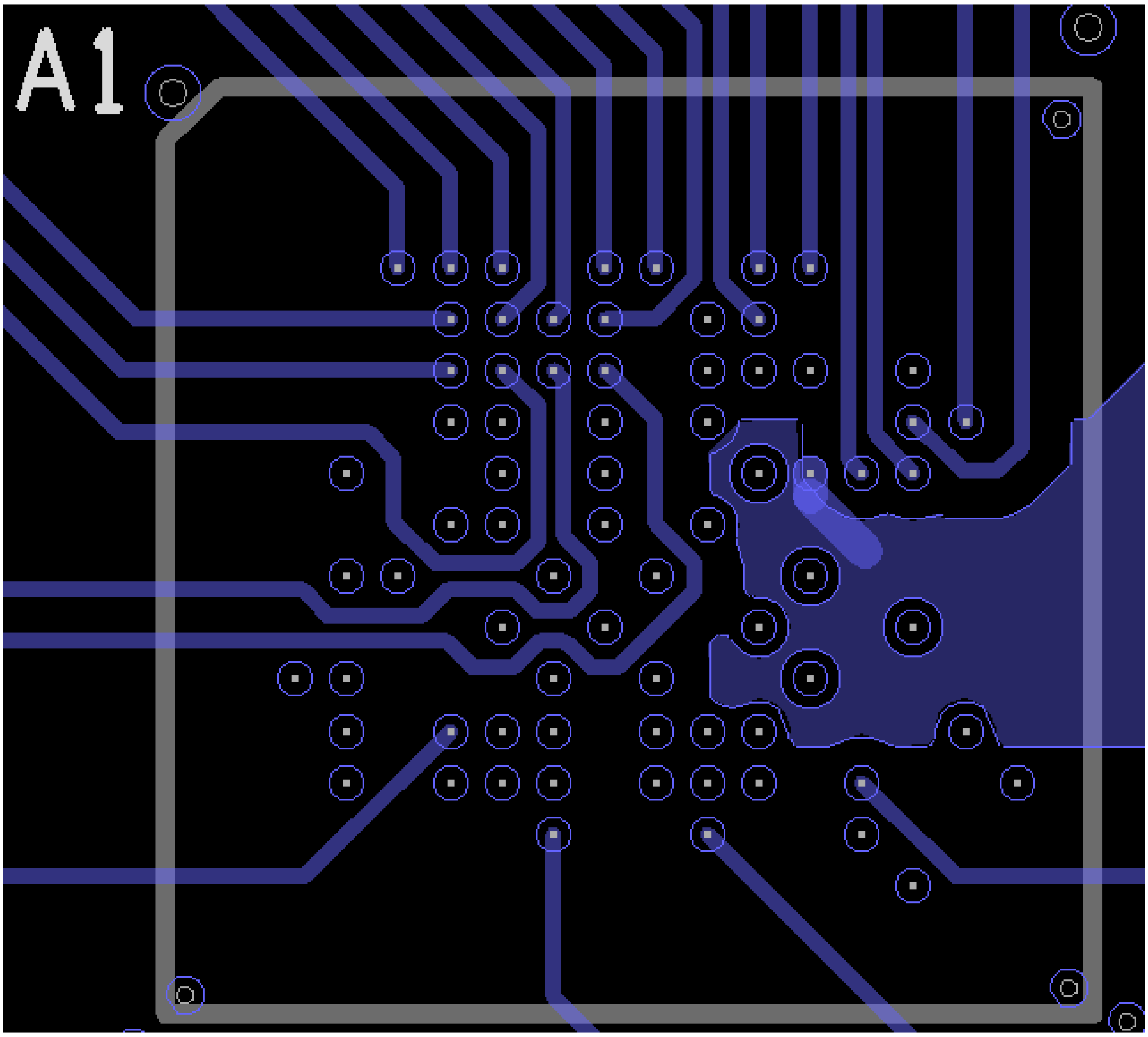


Figure 12 SSBG package corresponds to PCB middle layer routing diagram 2

(4) UWG

Compact series CPLDs currently have 3 types of UWG packages, namely UWG36, UWG49 and UWG81, with a pad pitch of 0.4mm. For specific package information, please refer to the corresponding chip package user guide of Unigroup.

UWG package has a small pitch between pads, and the space between pads cannot be routed (except for 2-layer flexible PCB boards). Blind and buried holes are generally required in PCB design.

Pad and via size recommendations are as follows:

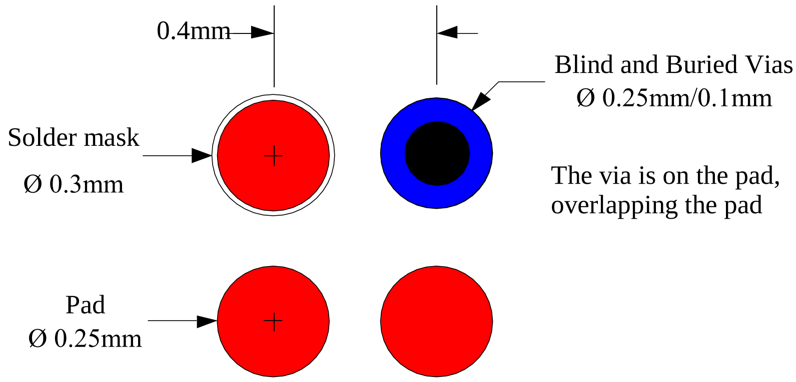


Figure 13 Schematic diagram of recommended dimensions for MBG package pads and vias

For UWG packaging, if a flexible board is used to design the PCB, the diameter of the pad is recommended to be 0.2mm (including solder mask and soldering layer are 0.2mm), and the width of the trace is recommended to be 0.06mm. The distance between the pad and the pad is 0.06mm. The trace of the power supply is appropriately widened after being drawn out. The principle of maintaining equal length and distance between the differential traces. It is recommended to add teardrops to the pad. On the PCB, the other side of the chip, steel sheets are required for reinforcement (draw a schematic diagram at the corresponding position and inform the PCB manufacturer). The PCB design example of UWG package is shown in the figure below.

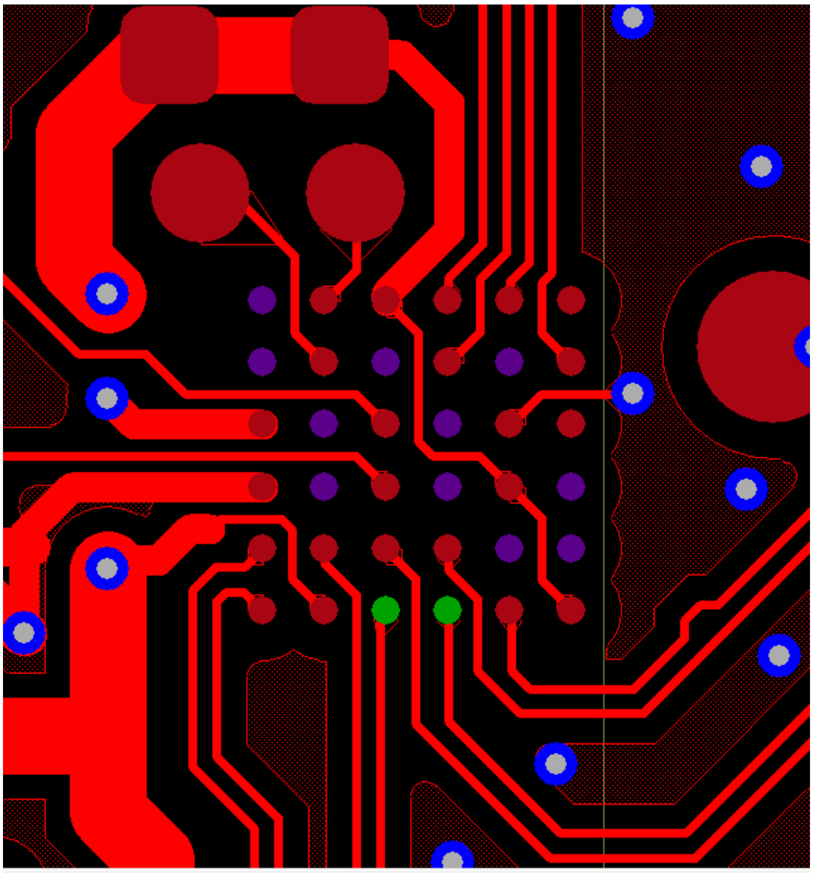


Figure 14 Schematic diagram of recommended dimensions for UWG package pads and vias

(5) LPG

Logos series FPGAs currently have two types of LPG packages, namely LPG100 and LPG144, and the spacing between the pads is 0.5mm. For specific package information, please refer to the corresponding chip package user guide of Tsinghua Unigroup.

The LPG package is square flat (QFP), and the PCB package and wiring can be designed according to the requirements of QFP.

4. Configuration

For related configuration information, please read Unigroup "UG030004_Compact Series CPLD Configuration (Configuration) User Guide" (please update to the latest version). In addition, there are pin descriptions in the chip package document.

(1) Instructions for use of pins

The chip pins have been detailed in the chip package document. The following table gives some instructions on the use of configuration pins that need special attention when doing single-board hardware design.

Table 4 Description of pins related to the configuration of Compact series CPLD chips

Pin name	Pin type	Instructions for use
INIT_FLAG_N	Multiplexed pins	When used as an initialization completion indication signal, it is recommended to pull up an external 4.7kΩ resistor to the power supply of the bank where it is located; Can not directly drive the indicator light, but can be driven by triode or MOS tube;
CFG_DONE	Multiplexed pins	When used as a configuration completion indication signal, it is recommended to pull up an external 4.7kΩ resistor to the power supply of the bank where it is located; It cannot directly drive the indicator light, but can be driven by a triode or MOS tube.
RSTN	Multiplexed pins	When used as a chip reset function, an external pull-up 4.7kΩ resistor must be connected to the power supply of the bank where it is located.
CFG_CLK	Multiplexed pins	When using the master SPI mode, an external pull-up 1kΩ resistor is required to the power supply of the bank where it resides.
TCK	Multiplexed pins	Requires an external pull-down 4.7kΩ resistor to ground.
JTAGEN	Multiplexed pins	When the JTAG interface is disabled, JTAGEN can be used as a dedicated pin. When JTAGEN input logic 1, the JTAG interface is enabled and used as a configuration interface. At this time, it is recommended to pull up an external 4.7kΩ resistor to the power supply of the bank; when When JTAGEN inputs logic 0, the 4 I/Os of the JTAG interface are used as user I/Os. An external pull-down 4.7kΩ resistor to ground is recommended.

(2) JTAG

The highest operating frequency of the TCK signal in JTAG is 50MHz, and an external 4.7kΩ resistor is required to be pulled down to the ground. When using a backplane or other situations where the JTAG signal needs to be divided into two, it is necessary to connect a resistor in series with TCK to reduce the stub pair signal As shown in Figure 15, resistors R1 and R2 are close to the signal bifurcation, and the resistance value can be determined according to the actual measurement results.

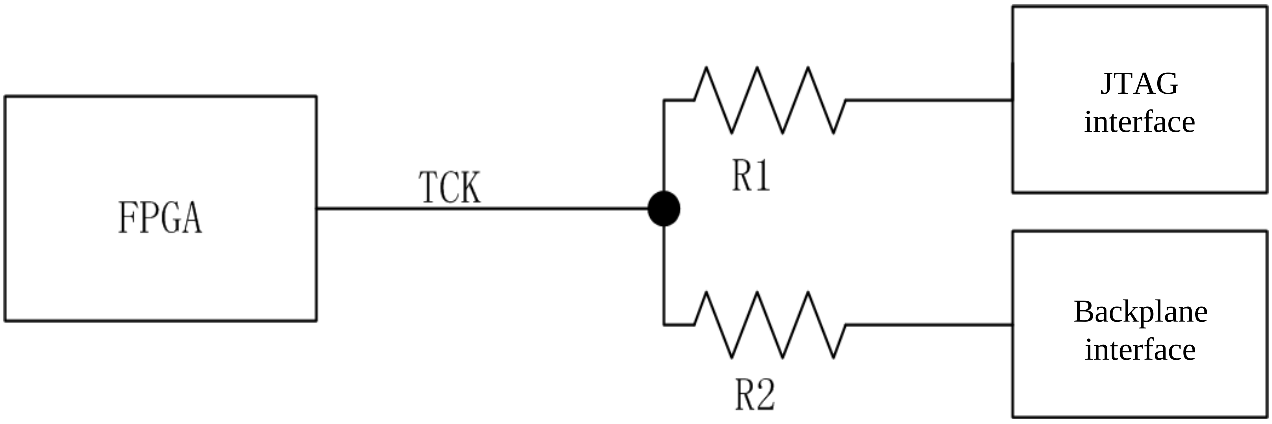


Figure 15 Schematic diagram of JTAG signal bifurcation resistors

(3) SPI

When using the SPI configuration mode, the precautions for the SCK signal of the SPI are the same as the TCK signal of the JTAG, and a resistor is connected in series at the source of the SCK.

When using the main SPI mode, the main clock CFG_CLK recommends an external pull-up 1kΩ resistor to the power supply of its bank, and the external Flash chip select signal FCS_N recommends an external pull-up 4.7kΩ resistor to the power supply of its bank, and pay attention to the bank where the SPI signal is located The voltage should be consistent with the voltage of the Flash chip (the voltage must meet the requirements of the Flash chip).

When using the slave SPI mode, it should be noted that the bank voltage where the SPI signal is located must be consistent with the interface level of the master device.

(4) Other configuration pins

Other commonly used configuration pins include RSTN, INIT_FLAG_N and CFG_DONE, etc. These pins are multiplexed pins, and the precautions for use are described in Table 4.

When multiplexed pins are used as ordinary IO, it is necessary to ensure that they are not affected by circuits other than the configuration circuit during power-on and configuration. It is recommended that they be used only for low-speed signal output.

The I2C configuration mode interface supports fast mode, which can be configured and reconfigured. SCL and SDA need an external pull-up resistor, and the recommended resistance is 2.2kΩ.

5. LVDS

(1) Chip pin selection requirements

When Compact series CPLD uses LVDS interface, the voltage of the bank where LVDS is located supports 3.3V/2.5V. Only bank0 supports LVDS true differential output. All banks support LVDS input, but only bank2 can provide internal differential terminal matching resistor 100Ω. "UG030005_Compact Series CPLD Input and Output Interface (IO) User Guide" for details.

(2) Other instructions

The LVDS level requirements of Compact series CPLDs are described in "DS03001_Compact Series CPLD Device Data Sheet".

(3) LVDS wiring requirements

1. After each pair of differential lines comes out from the chip pins, they should be as close to each other as possible, and the distance should remain unchanged;

2. The sending end and the receiving end should be as close as possible to make the LVDS trace the shortest, and use a 45° angle or an arc at the corner of the trace;

3. The differential trace impedance is controlled at 100 ohms ±10%. If there is an off-chip terminal matching resistor, the matching resistor needs to be close to the receiving end, and the distance to the receiving end pins should be minimized. The internal matching resistor of the receiving end should be used first;

4. The number of vias should be as small as possible, and it is recommended that each line has no more than 2 vias;

5. The wiring must have a complete reference plane, and the ground plane is given priority as a reference;

6. All differential pairs in the same group are routed on the same layer;

7. When the signal layer is changed, if the reference plane is changed at the same time, the reference plane needs to have layer-changing channel vias and be adjacent to the signal vias;

8. The spacing between different differential pairs should be greater than 5 times the line width, and the distance between the differential line and other signal lines should be greater than 5 times the line width;

9. The two lines in the differential pair are strictly equal in length, and the error is recommended not to exceed 5mil; the differential pair in the same group is equal in length, and the error is recommended not to exceed 20mil; the principle of error length compensation is where there is length difference compensation;

10. For long LVDS traces with speed transmission requirements, the loss of the traces can be optimized through simulation, especially the loss caused by impedance discontinuity at PCB vias and connectors.

6. MIPI

(1) Chip pin selection requirements

Compact series CPLDs support MIPI input and output.

MIPI_Ctrl is the MIPI high-performance application control pin. When it is connected to 2.5V or 3.3V, the device supports high-performance MIPI sending function; when it is connected to VSS or suspended, the device does not support high-performance MIPI sending function. This pin is available in PGC1KL\PGC2KL\PGC4KL series chips, but not in PGC1KG\PGC2KG\PGC4KD\PGC7KD series chips.

The MIPI input pin must select the odd differential pair in the differential order in Bank2 (because IDDRx4 is used in the recommended application, if IDDRx2 is used, this restriction is not necessary), the bank voltage is 1.2V. One-way HS can be realized by using MIPI level -MIPI input and bidirectional LP-MIPI. It is recommended to use a 2-wire scheme for the MIPI receiver. The unidirectional HS-MIPI input and bidirectional LP-MIPI share the same pair of I/O. At this time, the internal termination resistor of the chip is required. The figure is shown in the figure below. PCB traces are required to be processed in a differential manner.

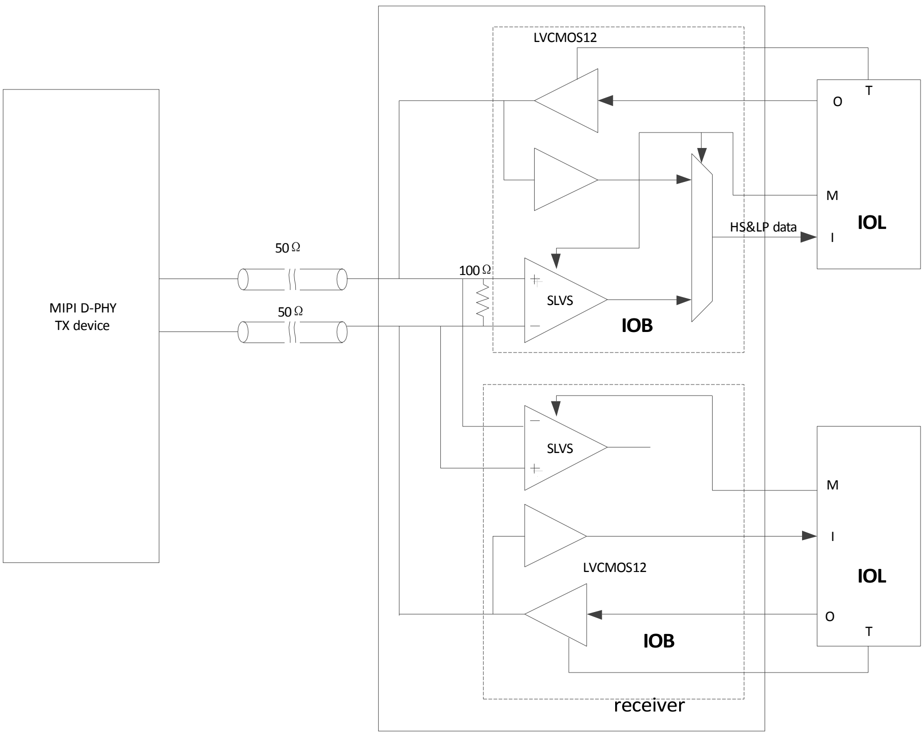


Figure 16 SLVS implements MIPI input (HS/LP)

The MIPI output of the Compact series CPLD uses LVCMOS25D level and external resistors, uses a 4-wire scheme, and realizes HS-MIPI output and LP-MIPI output through 4 I/Os. The 2 IOs corresponding to HS-MIPI output use LVCMOS25D level and are placed in Bank0, with a bank voltage 2.5V; 2 IOs corresponding to LP-MIPI output use LVCMOS12 level, which is a single-ended signal, matching resistors need to be placed in pairs to minimize the impact on differential wiring, corresponding to bank voltage 1.2 V. The principle block diagram is shown in the figure below:

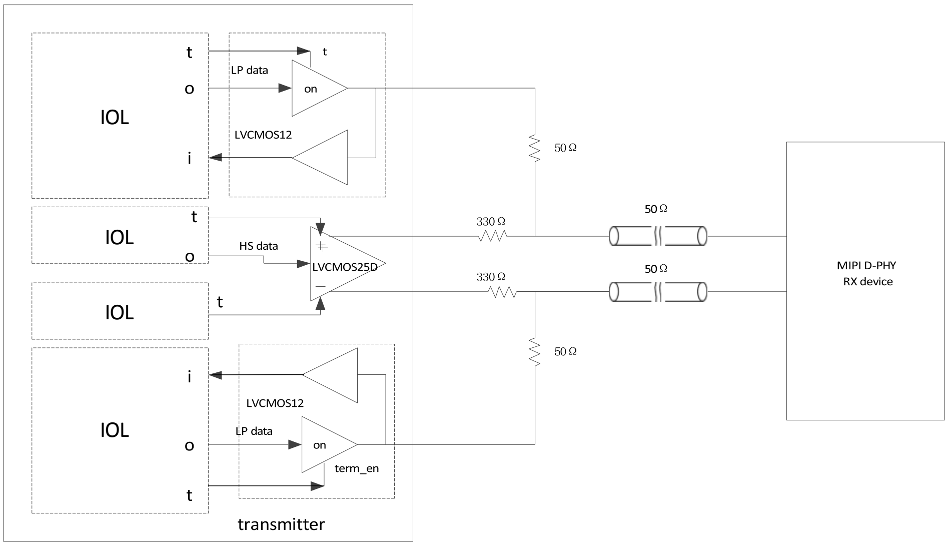


Figure 17 LVCMOS25D and external resistors for MIPI output (HS/LP)

(2) MIPI routing requirements

When wiring the PCB, the 50-ohm discrete resistors in Figure 17 should have the least impact on the differential lines, and the low-speed signals in the 4-wire solution should be routed according to ordinary single-ended signals. Other requirements are the same as the LVDS routing requirements.

7. Class Differential Output

In the application of Compact series CPLD, LVPECL33, MLVDS, LVDS25E and BLVDS level outputs need to be connected with external resistors to achieve differential output. "UG030005_Compact Series CPLD Input and Output Interface (IO) User Guide" has a block diagram and related instructions.

(1) Class differential output --- LVPECL33

LVPECL33 output is mainly used in point-to-point applications, and the most common application example is the clock distribution network on the board level. Figure 18 shows a possible implementation of LVPECL33 in point-to-point applications. The reference values given by RS and RP for 100Ω and 200Ω.

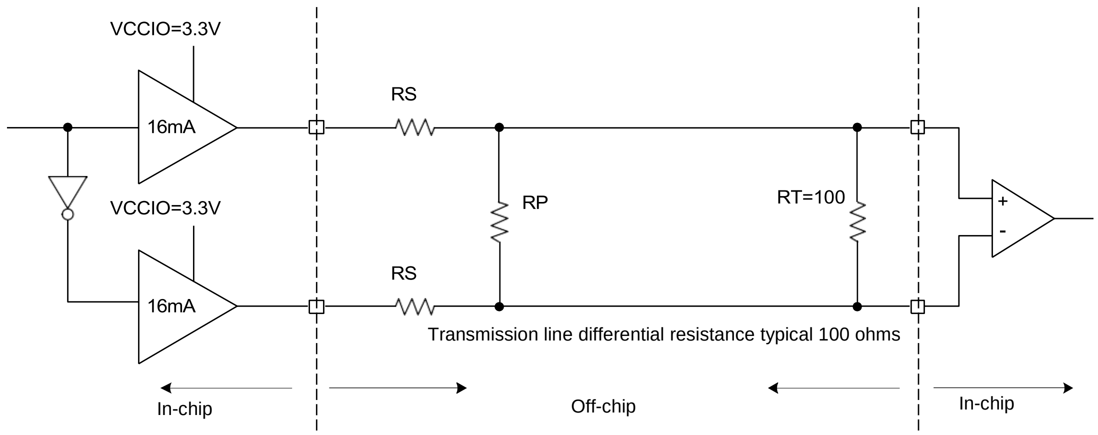


Figure 18 LVPECL point-to-point output example

(2) Class differential output---MLVDS25

MLVDS25 is used as a case where bidirectional multi-point drive output and input differential signals are required. I/O itself does not support this output standard, and it needs to be realized with the help of the complementary output principle of LVCMOS and the external resistance of the device. The differential amplitude of MLVDS25 is higher than that of BLVDS25 Large, and requires high current drive capability. Figure 19 shows the typical application of MLVDS25 multipoint configuration. The reference value of RS is 80Ω, the reference value of Rleft is 40-100Ω, and the reference value of Rright is 40-100Ω .

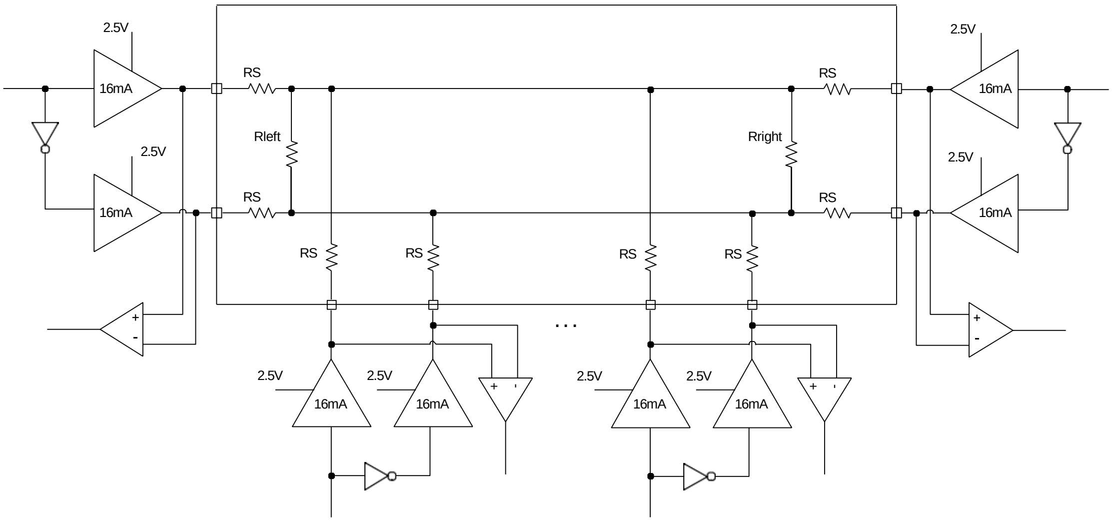


Figure 19 MLVDS25/BLVDS25 point-to-point output example

(3) Class differential output --- BLVDS25

BLVDS25 is an output standard similar to the MLVDS25 standard, and is also used as a situation where bidirectional multi-point drive output input differential signals are required. The difference between the two is that MLVDS25 is an industry standard, and the differential amplitude of MLVDS25 is larger than that of BLVDS25 , and requires high current drive capability. The implementation method is consistent with MLVDS25, and the circuit structure is shown in Figure 19.

(4) Class differential output --- LVDS25E

The 2.5V differential LVDS25E output is realized by LVCMOS complementary output. Figure 20 shows an example of an LVDS25E implementation. The reference value of RS is 150Ω, and the reference value of RP is 140Ω.

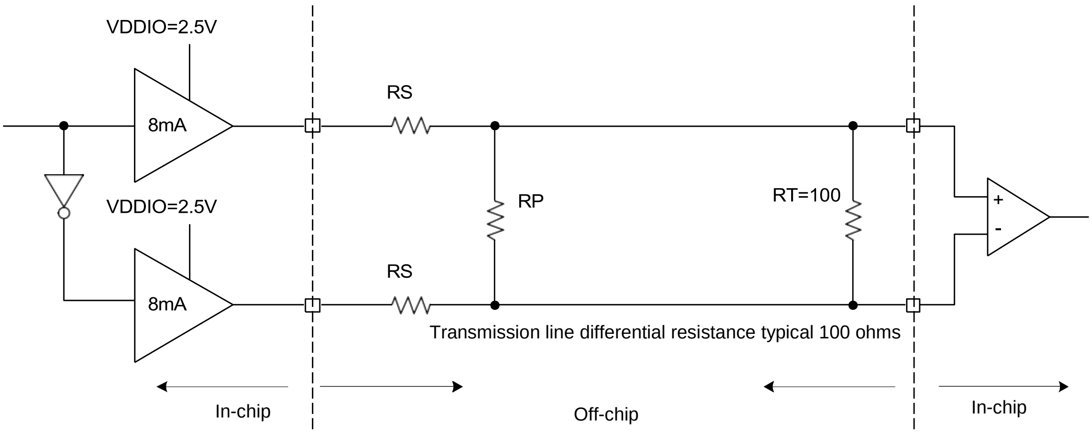


Figure 20 LVDS25E point-to-point output example

8. Clock

(1) Clock pin

Compact series CPLDs have a certain number of global clock input pins and PLL clock input pins, and support single-ended or differential input. For single-ended clock input, select the P terminal of the global clock differential pair to ensure that the clock signal goes through the global clock dedicated routing. The clock of the crystal oscillator and the reference clock input of general signals must enter these pins. The output reference clock does not need to be connected to these dedicated pins. At the same time, these pins can be used as ordinary I/O. The clock input pins can be referenced Pin descriptions in the package user manual.

(2) Clock routing

1. The active crystal oscillator drive power is filtered by a combination of magnetic beads and large and small capacitors;

2. The clock circuit is placed away from the edge of the board, and the wiring is far away from the general signal to avoid paralleling with other signal lines;

3. When the clock line is grounded, the grounded wire must be punched to the ground plane at a certain distance;

4. Clock traces must have a complete reference ground plane, and try to change layers as little as possible;

5. There must be ground vias adjacent to the clock vias, and there must be a complete reference ground plane after layer change;

6. The clock trace should keep the impedance continuous and avoid cross-segmentation;

7. A series resistor position is reserved at the source end of the clock line

9. Other Precautions

It is recommended that the user compile the project with the corresponding PDS software version after assigning the CPLD pins, and confirm whether the pin definitions are reasonable.

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